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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/762,572	01/23/2004	John Twynam	204552031600	3031

7590 01/25/2005

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EXAMINER	
LEE, EUGENE	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 01/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/762,572	TWYNAM, JOHN	
	Examiner	Art Unit	
	Eugene Lee	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/23/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, an insulating layer on the AlGanN layer (claim 3) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered. Neither Fig. 1 nor Fig. 4 show an insulating layer on AlGaN layer 14 nor 74 respectively.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claims 5 and 6 are objected to because of the following informalities: the limitations "each of the semiconductor is formed of a semiconductor having a C-plane Ga-surface" (claim 5) and "each of the semiconductor layers is formed of a C-plane Ga-surface oriented semiconductor" (claim 6) are being interpreted as the layers formed above the substrate but NOT the substrate itself. Appropriate clarification and/or correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 3 recites the limitation "AlGaN layer" in line 2 of said claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 2, and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khan et al. 5,192,987 in view of Yokogawa et al. 6,690,035 B1. Khan discloses (see, for example, FIG. 5) a transistor (compound semiconductor FET) comprising a buffer layer (AlN layer) 38, substrate 37; a plurality of III-N layer comprising GaN layer 39 and $Al_xGa_{1-x}N$ layer 41; source contact 43, drain contact 44, and gate contact 47. Khan does not disclose an n-type delta doped III-N layer. However, Yokogawa discloses (see, for example, FIG. 10) a MESFET comprising an active region wherein the active region comprises an undoped layer 22, and n-type doped layer (n-type delta doped III-N layer) 23. Yokogawa refers (see, for example, column 2, lines 15-62) to these layers as a first and second semiconductor layer (n-type delta doped III-N layer) wherein the second semiconductor layer has a higher concentration of impurities and a thinner film thickness. In column 20, lines 40-64, Yokogawa discloses the layers are grown epixtaxially from GaN. Further, in column 2, lines 59-62, Yokogawa discloses the first and second semiconductor layers achieve a low resistance value and high withstand voltage properties. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have an n-type delta doped III-N layer in order to achieve a low resistance value and high withstand properties.

Regarding the limitation "AlN layer" in line 2 of claim 1, see, for example, column 4, lines 19-20 wherein Khan discloses the buffer layer comprising aluminum nitride (AlN).

7. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Khan et al. '987 in view of Yokogawa et al. '035 B1 as applied to claims 1, 2, and 4 above, and further in view of Phillips 6,770,902 B2. Khan in view of Yokogawa does not disclose an insulating layer.

However, Phillips discloses (see, for example, figure) a transistor comprising a gate insulation layer 32. In column 5, lines 58-65, Phillips discloses that the gate insulation layer forms a MISFET instead of a Schottky contact. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have an insulating layer in order to form a MISFET instead of a Schottky contact.

8. Claims 5, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khan et al. '987 in view of Yokogawa et al. '035 B1 as applied to claims 1, 2, and 4 above, and further in view of Yamaguchi et al. 6,100,106. Khan in view of Yokogawa does not disclose each of the semiconductor layers being formed of a semiconductor having a C-plane Ga-surface. However, Yamaguchi discloses (see, for example, column 5, lines 27-39) a gallium nitride compound semiconductor device comprising a nitride semiconductor layer having a c-axis (C-plane) parallel to a substrate surface. In column 5, lines 32-36, Yamaguchi discloses that there is no reduction in the probability of recombination of electrons and holes, and low current density. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have each of the semiconductor layers being formed of a semiconductor having a C-plane Ga-surface in order to have no reduction in the probability of recombination of electrons and holes, and low current density.

Regarding the limitation "substrate is sapphire" in line 2 of claim 5, see, for example, column 2, lines 41-43, wherein Khan discloses the material of the substrate being sapphire.

Regarding lines 5-6 of claim 5, Khan in view of Yokogawa in view of Yamaguchi does not disclose the sheet doping concentration of the n-type delta doped III-N layer being within a

range of $1X10^{13}$ cm^{-2} to $2 X 10^{13}$ cm^{-2}." However, it was well within the skills of an artisan in the art to optimize the performance of a semiconductor device by adjusting the sheet doping concentration of a n-type delta doped III-N layer in order to achieve a low resistance value and high withstand voltage properties. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have sheet doping concentration of the n-type delta doped III-N layer is within a range of $1X10^{13}$ cm^{-2} to $2 X 10^{13}$ cm^{-2} because it was well within the skills of an artisan to optimize the performance of a semiconductor device by adjusting the sheet doping concentration in order to achieve a low resistance value and high withstand voltage properties. See In re Aller, 105 USPQ 233.

Regarding the limitation "substrate is SiC" in line 2 of claim 6, see, for example, column 6, lines 7-10, wherein Khan discloses the material of the substrate being silicon carbide (SiC).

Regarding lines 5-6 of claim 6, Khan in view of Yokogawa in view of Yamaguchi does not disclose the sheet doping concentration of the n-type delta doped III-N layer being within a range of $5X10^{12}$ cm^{-2} to $1.5 X 10^{13}$ cm^{-2}." However, it was well within the skills of an artisan in the art to optimize the performance of a semiconductor device by adjusting the sheet doping concentration of a n-type delta doped III-N layer in order to achieve a low resistance value and high withstand voltage properties. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have sheet doping concentration of the n-type delta doped III-N layer is within a range of $5X10^{12}$ cm^{-2} to $1.5 X 10^{13}$ cm^{-2} because it was well within the skills of an artisan to optimize the performance of a semiconductor device by adjusting the sheet doping concentration in order to achieve a low resistance value and high withstand voltage properties. See In re Aller, 105 USPQ 233.

Also, see column 20, lines 53-60, wherein Yokogawa discloses the first and semiconductor layers do not have to be a common material.

9. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Khan et al. '987 in view of Yokogawa et al. '035 B1 as applied to claims 1, 2, and 4 above, and further in view of Abrokwah et al. 5,895,929. Khan in view of Yokogawa does not disclose an electronic circuit provided with the compound semiconductor FET. However, Abrokwah discloses (see, for example, column 1, lines 15-46) FETS being part of electronic circuits such as logic and control circuits, high speed digital circuits, and the like. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have an electronic circuit provided with the compound semiconductor FET in order to integrate the transistors in more robust devices.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eugene Lee
January 22, 2005